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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,452	09/05/2003	Mark Ellsberry	44223-0100	8437

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,452	ELLSBERRY ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 - 6, 8,9,11,15,20,23,24,28 - 30, 41 - 43, 47 and 48* is/are allowed.

6)☒ Claim(s) *35,37,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1 - 6, 8, 9, 11, 15, 20, 23, 24, 28 - 30, 35, 37, 39 - 43 and 47 - 49.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on April 11, 2006 has been received and entered in the case.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 35, 37, 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosomi (U. S. Pat. No. 6,740,981) in view of Lo (U. S. Pat. No. 5,953,210).

Regarding claim 35, Hosomi discloses in e.g., Fig. 5 a chip-scale package (the packages in Fig. 5) comprising:

- a stack of substrates, each substrate (50A – 50D; column 10, lines 60 and 61) having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material; and
- a memory device (57A – 57D; column 10, line 56 and column 7, lines 38 – 39) on each substrate, each memory device having a first surface, the first surface of the memory device (57A – 57D) mounted facing the first surface of the substrate (50A – 50D), the memory device (57A – 57D) is electrically coupled to the substrate (see e.g., Fig. 5 and column 10, lines 56 – 59), the substrate (50A – 50D; ceramic) made from a different

material than the memory device (57A – 57D; single-crystal silicon) and having a coefficient of expansion that matches a coefficient of expansion of the memory device to within six parts per million per degree Celsius or less (The substrate of Hosomi is made by a ceramic, 6 – 8 ppm/°C, and the semiconductor die of Hosomi is made by a single-crystal silicon, 3.0 ppm/°C. Thus, the difference between the substrate and the die of Hosomi is within 6 ppm/°C. Therefore, Hosomi fully meets this limitation).

However, Hosomi does not disclose the five sides of the memory device being completely exposed and a sixth side of the memory device is partially exposed for improved heat dissipation. Lo teaches in e.g., Fig. 1 and column 3, lines 47 – 49 the five sides of a semiconductor die (40) being completely exposed and a sixth side of the semiconductor die (40) being partially exposed. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the underfill or protecting resin film from the memory devices of Hosomi as taught by Lo to provide an easy removal in the event of failure (column 3, lines 48 and 49). Furthermore, the limitation "for improved heat dissipation" is functional limitation which does not differentiate the claimed structure over Hosomi and Lo. In other words, the omission of the underfill or protecting resin film from the memory devices of Hosomi is able to improve heat dissipation of the memory semiconductor die even if it is not optimized for this purpose.

Regarding claim 37, Hosomi discloses in e.g., Fig. 5 a stackable chip-scale package (the packages in Fig. 5) comprising:

- a substrate (50A – 50D) having a first surface and an opposite second surface;

- a semiconductor device (57A – 57D) mounted on the first surface of the substrate using a plurality of electrical conductors (58A – 58D; column 11, lines 34 and 35), the semiconductor device (57A – 57D; column 11, lines 23 and 24) made from a different material than the substrate (50A – 50D; column 10, lines 60 and 61), the semiconductor device (57A – 57D) having a first surface, the first surface of the semiconductor device mounted facing the first surface of the substrate (see e.g., Fig. 5); and
- a plurality of solder balls (59) mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device (see e.g., Fig. 5), at least one of the solder balls electrically coupled to the semiconductor device (see e.g., Fig. 5).

However, Hosomi does not disclose the first surface of the semiconductor device remaining partially exposed and the other five surfaces of the semiconductor device being completely exposed for improved heat dissipation. Lo teaches in e.g., Fig. 1 and column 3, lines 47 – 49 the first surface of the semiconductor device (40) remaining partially exposed and five sides of a semiconductor die (40) being completely exposed. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the underfill or protecting resin film from the memory devices of Hosomi as taught by Lo to provide an easy removal in the event of failure (column 3, lines 48 and 49). Furthermore, the limitation "for improved heat dissipation" is functional limitation which does not differentiate the claimed structure over Hosomi and Lo. In other words, the omission of the underfill or protecting resin film from the memory devices of Hosomi is able to improve heat dissipation of the memory semiconductor die even if it is not optimized for this purpose.

Regarding claim 39, Hosomi discloses in e.g., Fig. 5 a memory module (5; column 9, lines 63 and 64) comprising:

- a main substrate (PCB; column 1, lines 41 – 44) with an interface to couple the memory module (5) to other devices (PC and PDA; column 1, lines 28 – 35); and
- a plurality of identical chip-scale packages (1 – 4; see e.g., Fig. 5 and column 11, lines 40 – 47) arranged in one or more stacks (see e.g., Fig. 5), each stack coupled to the main substrate (PCB), each chip-scale package (the package in Fig. 5) including
    - a substrate (50A – 50D; column 10, lines 60 and 61) having a first surface and an opposite second surface, and
    - a memory die (57A – 57D; column 10, line 56, column 7, lines 38 – 39 and column 11, lines 23 and 24) made from a different material than the substrate (50A – 50D; column 10, lines 60 and 61) and having a first surface (see e.g., Fig. 5), the first surface of the memory die mounted facing the first surface of the substrate (see e.g., Fig. 5).

However, Hosomi does not disclose the first surface of the semiconductor device remaining partially exposed and the other five surfaces of the semiconductor device being completely exposed for improved heat dissipation. Lo teaches in e.g., Fig. 1 and column 3, lines 47 – 49 the first surface of the semiconductor device (40) remaining partially exposed and five sides of a semiconductor die (40) being completely exposed. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to omit the underfill or protecting resin film from the memory devices of Hosomi as taught by Lo to provide an easy removal in the event of failure (column 3, lines 48 and 49). Furthermore, the limitation "for

improved heat dissipation" is functional limitation which does not differentiate the claimed structure over Hosomi and Lo. In other words, the omission of the underfill or protecting resin film from the memory devices of Hosomi is able to improve heat dissipation of the memory semiconductor die even if it is not optimized for this purpose.

Regarding claim 40, Hosomi discloses in e.g., Fig. 5 the chip-scale packages (the package in e.g., Fig. 5) in a stack have identical routing schemes (column 11, lines 40 – 47).

4. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hosomi and Lo as applied to claim 39 above, and further in view of Tokarsky (U. S. Pat. No. 4,698,267).

While Hosomi and Lo disclose the coefficient of expansion of the chip-scale package substrate (the substrate of Hosomi is made by a ceramic which has a range of the coefficient of expansion between 6 – 8 ppm/°C) being greater than the coefficient of expansion of the memory die (the semiconductor die of Hosomi is made by a single-crystal silicon which has the coefficient of expansion about 3.0 ppm/°C), Hosomi and Lo do not disclose the coefficient of expansion of the main substrate (PCB) being greater than the coefficient of expansion of the chip-scale package substrate. Tokarsky teaches in e.g., column 1, lines 18 – 33 a coefficient of expansion of a main substrate (PCB) being about 12 ppm/°C (this is greater than the coefficient of expansion of the memory die, 3.0 ppm/°C, of Hosomi). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the coefficient of expansion of the main substrate (PCB) of Tokarsky to be the specific coefficient of expansion of the main substrate (PCB) of Hosomi and Lo as taught by Tokarsky to avoid the breaking of electrical connections to the circuit board on thermal cycling (column 1, lines 21 – 23).

Furthermore, the following limitation "the coefficient of expansion of the chip-scale package substrate is selected such that the differential between a first interface thermal stress from the main substrate to a chip-scale package and a second interface thermal stress from the chip-scale package to the memory die is minimized so that the structural integrity of electrical joints at the first and second interfaces are retained" is functional limitation which does not differentiate the claimed structure over Hosomi, Lo and Tokarsky. In other words, since the PCB, the chip-scale package substrate and the memory die of Hosomi, Lo and Tokarsky have the selected coefficient of expansions as set forth in claim 49, the PCB, the chip-scale package substrate and the memory die are capable to minimize the interface thermal stresses and retain the structural integrity of electrical joints at the first and second interfaces even if they are not optimized for these purposes.

Allowable Subject Matter

5. Claims 1 – 6, 8, 9, 11, 15, 20, 23, 24, 28 – 30, 41 – 43, 47 and 48 are allowed.

6. The following is an examiner's statement of reasons for allowance:

Hayasaka et al. (U. S. Pat. No. 6,809,421) and Hosomi (U. S. Pat. No. 6,740,981) disclose one or more stacks of memory devices on a main substrate comprising a memory chip and a substrate. Also, the substrate has a coefficient of expansion that matches a coefficient of expansion of the memory semiconductor die to within six parts per million per degree Celsius or less. Kyougokuet al. (U. S. Pat. No. 5,995,379) discloses a staggered routing scheme in a stacked

semiconductor package. However, there is no reasonable suggestion or motivation to combine Hayasaka et al. and Hosomi with Kyougokuet al.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

7. Applicant's arguments filed on April 11, 2006 have been fully considered but they are either moot in light of the new grounds of rejection or are not persuasive.

On pages 11 – 13, applicant argues that Hosomi and Lo do not have motivation to combine their teachings because stack configuration of Hosomi effectively prevents removal of the semiconductors 57 from a substrate. This argument is not persuasive. Contrary to applicant's assertion and as stated in the rejection, motivation was established by Lo, specifically in column 3, lines 48 and 49 (to provide an easy removal in the event of failure). Furthermore, the omission of the underfill or protecting resin film from the substrate of Hosomi provides an easy removal of the semiconductor device in the event of failure during the semiconductor testing that is processed before or after stacking the substrates. In other words, the omission of the underfills or protecting resin films from the substrates of Hosomi are a well-known practice to one of ordinary skill in the art and the proposed modification is not change the principle of operation of Hosomi's device. Thus, the motivation is proper and Hosomi and Lo have motivation to combine their teachings.

Furthermore, applicant argues that the prior art of Hosomi and Lo fail to teach balancing of CTE values of these three components to balance the stresses perceived at these interfaces. This argument is not persuasive. Applicant should note that the features upon which applicant relies (i.e., balancing of CTE values of these three components to balance the stresses perceived at these interfaces) are not recited in the rejected claim 39. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Finally, the argument for the newly added claim 49, Hosomi, Lo and Tokarsky disclose the newly added claim 49 (see the paragraph four of this Office action for more detail).

For the above reasons, the rejection is maintained.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kresge et al. (U. S. Pat. No. 5,574,630) discloses in column 2, lines 66 and 67 that the coefficient of expansion of ceramic is 6 – 8 ppm/°C. Hirano et al. (U. S. Pub. No. 2003/0022464) discloses in page 1, section 0005, lines 16 – 18 that the coefficient of expansion of the single-crystal silicon is 3.0 ppm/°C.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Thursday, June 15, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER